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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/638,408	08/12/2003	Wei-Zen Chen	MR1035-1293	5164
4586	7590	05/18/2004	EXAMINER	
ROSENBERG, KLEIN & LEE 3458 ELLICOTT CENTER DRIVE-SUITE 101 ELLICOTT CITY, MD 21043				POKER, JENNIFER A
ART UNIT		PAPER NUMBER		
		2832		

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/638,408	Applicant(s) CHEN ET AL.
	Examiner Jennifer A. Poker	Art Unit 2832

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 12 August 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-11 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 12 August 2003 is/are: a) accepted or b) objected to by the Examiner.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

General Status

1. This is a first action on the merits of application filed on August 12, 2003. Claims 1-11 are pending and are being examined.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "*inter-metal dielectric layer*" (in claims 1, 9, and 10) "*the geometric conductive layer being circular*" (in claim 3) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a) because they fail to show/reference the "*inter-metal dielectric layer*" and "*the geometric conductive layer being circular*" as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 3 objected to because of the following informalities: applicant states, "...conductive layer is a circular." Examiner believes the term "a" was a typographical error and that the limitation should read, "...conductive layer is circular." Appropriate correction is required.
6. Claim 8 is objected to because of the following informalities: it recites the limitation "the size" in line 22. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.
7. Claim 9 is objected to because of the following informalities: it recites the limitation "the inside" in line 25. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.
9. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, applicant states, "...a plurality of conductive layers comprising at least one conductive line formed out of a symmetrical and geometric conductive layer..." This limitation is very confusing. Does the conductive layer comprise a conductive line, which forms a symmetrical and geometric shape?? Does the conductive line form the conductive layers, which are in a symmetrical and geometric shape?? Examiner understood this limitation to mean that the conductive layers comprise at least one conductive line, which forms a symmetrical and geometric shape on the conductive layer. Prior art was applied accordingly.

Regarding claim 4, applicant states, "...a tapped apparatus between the symmetrical stacked inductors." HOWEVER, claim 4 is dependant on claim 1, which only claims ONE symmetrical stacked inductor (preamble). Based on wording of claim 4, examiner is not sure of the location of the tapped apparatus. Therefore, examiner will assume, for purposes of examination, that the tapped apparatus is connected to the stacked inductor. Prior art was applied accordingly.

Regarding claim 8, applicant states, "even conductive layer is not the same size of the odd conductive layer." It is not clear what layers are odds and evens. Examiner understands that alternating layers are odds and evens. Therefore, the bottom layer would be odd, the second layer is even, third layer is odd, etc. Prior art was applied accordingly.

Regarding claim 9, applicant states, "...an inside even conductive layer being the same as the symmetrical and geometric odd conductive layer..." This limitation is indefinite. Examiner does not know what applicant means by claiming, "being the same as". Examiner assumes applicant means same size/shape. Prior art was applied accordingly.

10. Claims 8-10 recite the limitations "the even conductive layers and "the odd conductive layers". There is insufficient antecedent basis for this limitation in the claim. Examiner does not know what layers applicant intends to be odd or even. Correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1, 2, 4, 7, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 6,611,188 to Yeo, et al.

Regarding claims 1 and 2, Yeo, et al, discloses a multilevel interconnected integrated vertical inductor wherein each inductor comprises:

- (1) conductive lines, which form a plurality of conductive layers (22, 24, 26, 28, 30, 32 and 34) forming a symmetrical and geometrical shape (figures 2a, 6a; column 8, lines 55-60);
- (2) a dielectric that is deposited between the adjacent layers of conductive material (column 9, lines 23-24);
- (3) vias for the extension of the vertical conductors (21, 23, 25, 27, 29, and 31) (figures 2a, 6a; column 9, lines 32-34, 53-55);

It can be seen in figure 2a that the conducting lines of the layers do not intersect and the lines are generally of rectangular shape.

Regarding claim 4, Yeo, et al, further discloses input/output connectors 22' and 23' being created in desired locations of the inductor (column 9, lines 55-56; figure 2a). Because the general definitions of "tapped" based on *The American Heritage® Dictionary of the English Language, Fourth Edition* Copyright © 2000 by Houghton Mifflin Company is:

- (a) to make a physical connection with or open outlets from;
- (b) to establish an electric connection in (a power line), as to divert current secretly;
- (c) to establish access to or a connection with;

it was understood that the creations of connectors (22' and 23') would be sufficient for that of a "tapped" apparatus.

Regarding claim 7, Yeo, et al, further discloses that a conductive material forms the body of the inductor (column 9, lines 1 and 2). Furthermore, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ

Regarding claim 8, Yeo, et al, further illustrates in figure 2a that the size of alternating conductive layers are not equal.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being obvious over U.S. Patent Number 6,611,188 to Yeo, et al.

Regarding claim 3, Yeo, et al, discloses the claimed invention except for circular shape of the conductive layer. Yeo, et al, does however disclose a square/rectangular shape. It would have been obvious to one having ordinary skill in the art to utilize any suitable shape for the conductive layer, since applicant has not disclosed that the circular shape solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with any shape.

Regarding claims 5 and 6, Yeo, et al, discloses the multilevel interconnected vertical inductor, but does not state that it is used to form a single chip transformer (claim 5) or used to form a single chip balun element (claim 6). It has been held that a recitation with respect of the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647

15. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 6,611,188 to Yeo, et al. in view of U.S. Patent Number 5,610,433 to Merrill, et al.

Regarding claim 9, Yeo, et al, discloses the claimed invention except for an inside even conductive layer.

Regarding claim 10, Yeo, et al, discloses the claimed invention except for an outside odd conductive layer.

Regarding claim 11, Yeo, et al, discloses the claimed invention except for the use of two conductive lines per layer.

Merrill, et al, discloses a multi-turn, multi-level inductor comprising two lines per conductive layer. As can be seen in figure 1, it can be interpreted that the top layer is odd and the middle layer

is even. Both layers have two conductive segments, an inner and outer segment. The inner segment of the middle (even) layer is the same size as that of the inner segment of the top (odd) layer, and is connected by vias to the inner segment of the top (odd) layer. The even conductive line does not intersect with the inside conductive line. Furthermore, an outer segment of the top (odd) layer is the same size as that of the middle (even) conductive line and is connected to the outer segment of the middle (even) layer. The odd conductive line does not intersect with the outside odd conductive line. The odd and even (top and middle) layers are all parallel). A structure as described above, is used to obtain a high value inductor with a high Q factor (column 1, lines 54-62).

One skilled in the art, at the time the invention was made would have found it obvious to combine the teachings of Yeo, et al, with the teachings of Merrill, et al and incorporate more than one conductive coil/line per layer and connect inner and outer lines in order to obtain a high value inductor with a high Q factor.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer A. Poker whose telephone number is 571-272-1997. The examiner can normally be reached on 5:30-4:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin G. Enad can be reached on 571-272-1990. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jap
May 14, 2004

[Handwritten Signature]
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